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This is the Final Report of the research conducted at Stanford Electronics Laboratories under the sponsorship of the Joint Services Electronics Program from March 1, 1994 through March 31, 1997. This report summarizes the area of pbulciations and presentaions sponsored by the contract DAAH04-94-G-0058.

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JSEP FINAL REPORT

Period of March 1, 1994 - March 31, 1997

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Joint Services Electronic Program
(U.S. Army, U.S. Navy and U.S. Air Force)
Contract DAAH04-94-G-0058

J. S. Harris
Principal Investigator
Program Director

Monitored by U.S. Army Research Office

Abstract

This is the final report of the research conducted at Stanford Electronics Laboratories under the sponsorship of the Joint Services Electronics Program from March 1, 1994 through March 31, 1997. This report summarizes the areas of research, identifies the most significant results and lists the dissertations, publications and presentations sponsored by the contract (DAAH04-94-G-0058).

Key Words and Phrases: None

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1. INTRODUCTION

This report summarizes the activities in the research programs at the Stanford Electronics Laboratories sponsored by the Joint Services Electronics Program under contract DAAH04-94-G-0058. This contract is monitored by the Army Research Office, Research Triangle Park, North Carolina.

This report covers a period of significant change in the Stanford JSEP program as two initial projects were new, and during the course of the three year program, two projects were discontinued and two changed emphasis. Thus, by the completion of the program, there was greater than a 50% change in the research projects. This was a reflection of reality as the budget was reduced and a desire to insure a vital program by seeding new ideas and projects which could potentially lead to larger programs with conventional DoD funding. The value of JSEP is to provide early stage funding of new ideas with leverage to create entirely new programs. This often takes two or more years to proceed through the DoD proposal process and the JSEP flexibility provides great leverage in seeding such new ideas in the interim period when virtually nothing would otherwise occur.

The research program is divided into two main areas:

- Semiconductor Materials, Processes and Circuits
- Information Systems

The work units and tasks within each of the above areas are summarized below, together with the investigator responsible for the unit.

1. Semiconductor Materials, Processes and Circuits
   a. Investigation of Transport in Quantum Dots (J. S. Harris)
   b. Physics and Applications of Ultra-Small Structures (R. F. W. Pease)
   c. Investigation of a Metal Source and Drain Field Emission Transistor (C. R. Helms)
   d. The Electronic Structure and Interfacial Properties of High Temperature Superconductors (W. E. Spicer)
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2. Information Systems

   a. Portable Video on Demand in Wireless Communication (T. H. Meng)
   b. Wireless Data Transmission Fundamentals (J. M. Cioffi)
   b. Smart Antennas for Mobile Radio Networks (T. Kailath)
   c. Efficient Data Compression (T. Cover)

2. SIGNIFICANT RESULTS

The most significant accomplishments during this contract, as determined by the JSEP Director, are summarized below.

- *Transport in Quantum Dots*

The first well resolved energy spectrum of a semiconductor quantum dot was mapped out from transport measurements as a function of magnetic field. The energy levels participating in the electron transport were identified by the unique 'fingerprint' in magnetic field displayed by the motion in energy of each level. This identification permitted comparison of the spectrum for the dot under changing external conditions such as shape, size and number of electrons in the dot. Most significantly, initial experimental results showed almost identical energy spectra for successive electron occupancy in the dot, in good agreement with a single particle model of the quantum dot.

- *Si Nanopillars*

Fabrication of quantum structures with precise uniform dimensions is required to exploit quantum size effects is semiconductor devices. A combination of e-beam lithography, etching, strain effects and oxidation have been used to fabricate Si nanopillars. Single nanopillars have been isolated and spin-on glass used to planarize the structures and apply ohmic contacts. Current vs. voltage measurements have been made on single pillars. Such structures are the first step in the development of nanometer scaled pillar or surround gate MOSFETs.

- *Portable Video on Demand*

Low power video compression is absolutely essential to provide video information to the mobile battlefield warrior of the future. This project focused on both the algorithm and circuit design techniques to implement low-power video compression/decompression at power levels two orders of magnitude below existing solutions. This low-power video compression system not only provides a compression efficiency similar to industry standards, but also maintains a high degree of error tolerance to guard against the transmission errors encountered in wireless communication. A hardware prototype video decoding chip set was developed for decompressing full-motion video transmitted through a wireless link at less than 10 mW.

- *Wireless Data Transmission Fundamentals*

Establishing the bounds for the highest possible data transmission rate in fixed and portable wireless digital transmission environments is critical in developing useful wireless system architectures. A new class of codes and design criteria/procedures were realized that evaluate the wireless environment, producing a number of codes that allow the highest data rates to be obtained on a wireless point-to-point link.

3. SEMICONDUCTOR MATERIALS, PROCESSES AND CIRCUITS

3.1 Investigation of Transport in Quantum Dots

Scientific Objective

A full understanding of transport in quantum dots will be required in any successful implementation of single electron electronics. In particular, most studies of quantum devices have concentrated on the very low bias equilibrium behavior; we concentrate instead on the technologically relevant non-linear high bias operating regime. We had two main objectives: 1) to study the fundamental characteristics of coulomb blockade and charge coupling in transport through quantum dot arrays, and 2) to understand the mechanisms controlling electron transport through single quantum point contacts and quantum dots.

Summary of Research

We previously reported initial investigations of the electronic transport through 200 x 200 two dimensional quantum dot arrays patterned on a molecular beam epitaxy (MBE) grown GaAs/AlGaAs heterostructure. The current-voltage (I-V) relation of the arrays showed two striking features: a threshold for conduction, and multiple switching events accompanied by a hierarchy of hysteresis loops. By changing the voltage applied to a single Schottky gate deposited over the entire array, it was possible to move between the hysteretic and non-hysteretic regimes. We continued this investigation by focusing on the mechanisms responsible for the switching and hysteresis in single point contacts and quantum dots. It is this behavior, and control of it, that will be most relevant in any technological application.

Our investigation extended into a more detailed analysis of single quantum dot electrical transport, in an effort to understand and control the quantum transport mechanisms present in the large bias regime. Third generation split-gate devices were fabricated with a design optimized for this study. The continued experimental effort has produced new results and new understanding of the energy level structure and thus the quantum transport through these quantum dot structures. Most significantly, the results give insight into the level and applicability of different models used to describe the electrical characteristics. Accurate but cost effective (minimal sophistication that is required) modelling of the quantum dot transport is a necessary condition before circuit design will be possible for integrated quantum dot architectures.

All devices measured were fabricated by lithographically patterning a GaAs/AlGaAs epitaxially grown heterostructure. We utilized a standard modulation doped architecture to create a two dimensional electron gas (2DEG) approximately 800 Å below the wafer surface. First generation and second generation split gate devices were fabricated from MBE material

grown in our laboratory with a mobility and sheet density of ≈200 000 cm^2/Vs and $3.5x10^{11}$ cm^{-2}; second generation etched devices were patterned on CVD material grown at Sandia National Labs by our collaborator H.Chui with a mobility and density of ≈300 000 cm^2/Vs and $2.0x10^{11}$ cm^{-2}. Third generation split gate devices for the detailed energy structure investigations were again fabricated on MBE material grown in our laboratory, with similar material parameters to those listed above.

The devices were formed using electron-beam lithography to define the point contact, dot and array features. Minimum feature size was 100 nm, point contact barrier openings were 200-400 nm, and the array periodicity was 800 nm. This lithographic pattern was used as a mask for wet chemical etching 800 Å deep through the 2DEG in the case of etched structures, or NiCrAu metal gate evaporation for the split gate devices. A single 1000 Å Au front gate was deposited over the etched devices. A ground plane below the mounted chips was used as a back gate.

In the large arrays discontinuous and hysteretic jumps in the current were measured in all devices. All hysteresis loops observed were traversed in a counter clockwise direction in I versus V. Multiple hysteresis loops shrunk and dissociated into smaller loops as the temperature was raised. The arrays also showed a voltage threshold for conduction, below which zero current flowed. These results have been described in a previous JSEP Annual Report.

The second effort focused on single point contact and quantum dot devices. All of these structures showed one bistable switching region as the dc conductance jumps from zero to a finite value, typically $(60\ k\Omega)^{-1}$. The conductance switched between two bistable states over a small voltage range as the devices turned on. Applying a constant source drain voltage to bias the device at some midpoint of the switching region yielded a random telegraph signal in the current as a function of time. The clean hysteresis loops initially observed in the arrays can thus be described as bistable conductance regions with average bistable state lifetimes » measurement sweep rate. In the long switching time or 'hysteretic' regime, we used the front and back gates to control the size and position of the hysteresis. As an increasingly negative backgate voltage was applied, the hysteresis loop expanded in size and the initial turn on threshold shifted to higher source-drain bias. In the short switching time or telegraph noise regime we achieved a significant result; application of a small backgate voltage changed the average state lifetimes dramatically, and thus controlled the hysteresis behavior. The CVD etched devices extended the temperature range of this behavior to above 4.2K.

The third generation quantum dots were used to study in more depth the high bias transport through a quantum dot and the relationship between the measured experimental energy level structure and the theoretical structure and transport predicted by various quantum

mechanical models. In the first well resolved measurement of this kind on a semiconductor quantum dot, the energy spectrum of the dot was mapped out as a function of magnetic field. The energy levels participating in the electron transport were identified by the unique 'fingerprint' in magnetic field displayed by the motion in energy of each level. This identification permitted comparison of the spectrum for the dot under changing external conditions such as shape, size and number of electrons in the dot. This behavior was then used as a direct link to the quantum mechanical models that describe transport through quantum dots. Most significantly, initial experimental results showed almost identical energy spectra for successive electron occupancy in the dot, in good agreement with a single particle model of the quantum dot. Closer investigation has also revealed spectral features that require more detailed Hartree-Fock and numeric many-body models. In this way the energy spectroscopy will help guide both future device design and perhaps more importantly, device modelling.

3.2 Physics and Applications of Ultra-small Structures

Scientific Objective

The main scientific objective of this study is to obtain precise electrical, optical and structural information from controlled nanostructures to provide an understanding of the intrinsic electronic properties of nanostructures and determine possibilities for their application to novel, advanced devices.

Summary of Research

There are two main areas of research within this study:

1) The low-current behavior of liquid metal ion sources
2) Device applications of silicon nanopillars

1) The low-current behavior of liquid metal ion sources

Liquid metal ion sources (LMIS) provide a unique source for finely focused ion beams of various metals that can be used in a variety of micro- and nanofabrication applications. These include lithography, localized etching and deposition, localized doping, microscopy, and sample preparation for microscopy. However, the performance of current ion beam machines is limited by the large energy spread of the ions which is largely a result of ion-ion interaction just outside the LMIS. If the current from the source could be reduced, the energy spread would be reduced, resulting in a net improvement in the overall machine performance. However, LMIS sources, for reasons previously not well understood, shut off or pulse below some minimum current. The goal of this work is to develop a theory that explains this behaviour and verify the model with experimental results. Once the phenomenon is clearly understood, it may be possible to identify sources or operating techniques for improving the characteristics of LMIS.

A model has been developed to describe the minimum emission current from LMIS. It is based on balancing the metal flow rate within the bulk of the LMIS with the evaporation/ionization rate from the surface of the LMIS. The model predicts that the minimum current is independent of the radius of the underlying tungsten needle, which has been confirmed experimentally. Model predictions of the minimum current from a gallium LMIS of 438 nA at 33°C match almost exactly with the experimental value of 437 nA. Using this model, a variety of different source metals were surveyed to identify those which might have significantly lower minimum currents. Bismuth appeared to be the most attractive candidate with a predicted minimum current of 38 nA. Attempts to fabricate a bismuth LMIS were only partly successful, due to difficulties in getting the bismuth to wet a tungsten needle. Nonetheless, some emission was observed from a bismuth source with a minimum current <77 nA, thus confirming that the model can be used to predict trends if not actual numbers.

Based on this model, a number of future research opportunities have been identified. A tin source should provide somewhat better characteristics than the conventional gallium source. If a technique could be found to reduce the surface tension of the metal, perhaps through the use of certain alloys, then the minimum current could be significantly reduced. Finally, if emission could be achieved without the formation of a Tayler cone, perhaps by restricting the liquid metal supply, then there would be no limit on the minimum emission current.

2) Device applications of silicon nanopillars

The goal of this project is to study the electrical characteristics of silicon nanopillars as they relate to devices such as the pillar field effect transistor and the single electron transistor. Two terminal current versus voltage measurements yield information about the pillar structure and the effect of strain at the silicon/silicon dioxide interface. Planned addition of a surrounding gate will improve these measurements and form a transistor. Current has been measured between the top and bottom of silicon nanopillars but does not yield conclusive results about the pillar's conductive properties. Redesigned samples will separate the factors affecting pillar current.

Structures under investigation are silicon/silicon nitride multilayer nanopillars with electrical contacts at top and bottom. The nanopillars are created by masked reactive ion etching and self-limited lateral oxidation of a multilayer substrate. The multilayers are alternating layers of deposited polysilicon and thermal silicon nitride, the silicon nitride grown 1 nm thick in a rapid thermal annealer. The potential application of single electron charging effects and coulomb blockade prompted fabrication of pillars with two silicon nitride layers, acting as tunnel junctions, above and below a polysilicon island. Future work will include addition of a surrounding gate to make a three terminal device. The silicon core of the pillar is 15 nm wide. Electrical contact to the pillar top requires removal of the cladding oxide, so a

dielectric planarization and etch back process exposes the top of each nanopillar's silicon core while leaving the lower section insulated. Patterned aluminum on titanium tungsten makes electrical contact to the pillar top, and aluminum on the backside of the doped substrate forms the bottom contact.

Two terminal current versus voltage measurements of single and multiple identical multilayer pillars show nanoamp sized current uncorrelated to the number of pillars. Arrays of one and 512 pillars with tunnel junctions both showed similar current characteristics with a roughly exponential turn-on at ± 1 V. The data suggest that high tunnel junction and contact resistances plus leakage current through the planarizing dielectric are present in the structures. High tunnel junction and contact resistance means that little of the measured current flows through the pillars, making the number of pillars simultaneously measured irrelevant. The current instead flows between the large top contact and the substrate through the planarizing dielectric.

Samples in progress will show reduced contact and pillar resistance with less dielectric leakage, giving more descriptive current versus voltage data. New samples are designed for measuring total pillar current, contact resistance, and dielectric leakage current independently. Pillars are made from single crystal silicon, which eliminates tunnel junction resistance, and contacts are made of only aluminum, which reduces contact resistance. Most importantly, higher quality planarizing dielectric will reduce leakage current. Planarization was originally accomplished with spin on glass, a material providing decent planarity but poor insulating properties. Deposited low temperature oxide is a better insulator, but deposition is conformal above the pillars. A resist etch back technique is used to transfer the planar surface of spun photoresist onto the underlying deposited oxide. Etching the resist on oxide in a plasma balanced for equal etch rates gives a planar etch front. The etch is stopped when 50 nm of silicon pillar core is exposed, ready for metallization. The new samples, with simpler pillars and contacts plus a better dielectric, should allow the extraction of pillar current from the combined effects of pillars, contacts, and dielectric leakage.

3.3 Investigation of a Metal Source and Drain Field Emission Transistor

Scientific Objective

The objective of this project was to investigate the potential advantages of metal source and drain Metal-Oxide-Semiconductor-Field-Effect-Transistors (MOSFETs) over conventional (doped source and drain) MOSFETs including; ease of fabrication and unconditional immunity to parasitic bipolar and latch-up effects.

Summary of Research

Initial metal source drain MOSFETs proved to be poor performers compared to similarly sized conventional MOSFETs. The lower drive current in the 'on' state was attributed to the presence of a finite 'gap' between the edge of the poly gate and the edge of the platinum silicide (PtSi) source metal. The much higher leakage currents in the 'off' state originate at the drain end of the device, where electric fields cause thermally assisted field emission of electrons from the drain into the silicon. Insight into these leakage problems can be attained by examing the low temperature characteristics of these devices.

Simulations on metal source drain MOSFETs have shown acceptable drive current and short channel effects in devices with channel lengths down to 0.025 μm. The scalability of these metal source and drain devices is particularly impressive at low temperatures (77° K), as described by Tucker. It seems possible in light of these recent studies to build a metal source and drain device that has all the advantages previously mentioned, as well as superior scalability to well below 0.1 μm and free of the low drive and high leakage current problems.

We carried out the first detailed experimental investigation of the low temperature, field emission characteristics of PtSi source and drain MOSFETs. The I-V characteristics were measured at various temperatures down to 4.2° K and for channel lengths down to 1 μm. Device fabrication was optimized so that it is free from the 'gap' at the poly edge described earlier. We observe a definite transition in the current flow mechanism from thermal to field emission as the temperature is reduced below 100° K. In this low temperature 'field emission mode', the drive current when the device is 'on' is comparable to that of a conventional MOSFET, and short channel effects are not observable down to 1 μm, despite the fact that the substrate is nominally undoped. For temperatures less than about 100° K, all significant current flow (> 0.1 pA) occurs by the process of field emission and the device is being operated in the 'field emission mode'. The field emission characteristic is largely independent of temperature. The Schottky barrier alone is responsible for preventing the flow of current into the channel and thus it is clear why substrate doping is not required.

A full 2-D Poisson solver was developed and integrated with first principles tunneling calculations in order to theoretically examine the effects of device geometry (tip sharpness, channel length, and gate oxide thickness) and materials and system parameters (Schottky barrier height and temperature) on the hole and electron field emission characteristics. The subthreshold slopes of these characteristics were found to decrease monotonically with gate oxide thickness with no theoretical limit. This is in contrast to the theoretical limit, defined by temperature, that exists for the subthreshold region of a conventional MOSFET. Subthreshold current levels were also found to be generally smaller than those of conventional devices by several orders of magnitude. Shallow source/drain junctions with sharp tips were found to be

optimal in terms of promoting hole field emission drive currents and controlling Drain-Induced-Barrier-Thinning (DIBT) hole leakage currents. Low barrier heights (for good drive currents) and low temperatures (for low leakage over the low barrier) were also found to be optimal.

3.4 The Electronic Structure and Interfacial Properties of High Temperature Superconductors

Scientific Objective

The electron/hole concentration in high temperature superconductors (HTSCs) is understood to play a central role in the behavior of these new materials. The primary focus of this research was to investigate the electronic structure issues of HTSCs by varying the density of the materials.

Summary of Research

Two forms of carrier concentration modification were used -- oxygen depletion and cation substitution. The oxygen depleted samples were created by annealing in argon which resulted in fewer hole carriers. The cation substituted samples also reduced the hole concentration but in this case by substituting Dy^{3+} for Ca^{2+}. The cation substituted samples complimented the oxygen reduced samples in that the doping range was larger with the cation samples while the dopant location with respect to the carrier layers was optimal in the oxygen reduced samples. Both types of samples gave similar results.

The electronic structure gradually exhibited the symmetry of a double-sized, 45° rotated lattice as the hole concentration was reduced. This is consistent with increased electron-electron correlation particularly the electron spin as the electron concentration was pushed toward the Mott-insulating, half-filled, antiferromagnetic state. This trend increased monotonically with decreased hole concentration. This trend is consistent with an explanation of HTSCs where the coupling of carriers is at least partially mediated by spin-spin correlations. Other researchers have observed this new symmetry and noted its disappearance at higher temperatures. Still others have noted that at very high hole concentrations (where spin-spin correlations decrease), superconductivity is quenched. The peak in superconducting critical temperature versus doping can be described as the overlapping of two curves where different effects dominate. At lower hole concentrations, the correlations necessary for HTSC are promoted at the expense of absolute hole concentration. With so few holes in the system, interactions to form pairs are infrequent due to sheer scarcity. As the hole concentration is increased, the T_c also increases toward an optimum value beyond which the decrease in spin-spin correlations causes the T_c to again fall. The data from this study has contributed in a significant way to the understanding of HTSCs.

3.5 On-Chip Thin Film Solid State Micro-Battery

Scientific Objective

The objective of this work is to develop the fabrication technology and characterize the performance of thin film solid state micro-batteries that are suitable for monolithic integration with semiconductor integrated circuits.

Summary of Research

Integration of solid state micro-batteries onto integrated circuits will offer several advantages. (1) The micro-batteries can directly replace bulk batteries in portable electronic systems. In addition to the reduction in weight and size, each IC will have its own battery, and hence the total charge capacity of the system could be much higher than that available from a single set of batteries. (2) The micro-battery can provide a backup energy source for non-volatile storage and continuous operation. (3)The micro-battery is more effective than a de-coupling capacitor in regulating the power supply level on the chip. A stable supply level is especially critical for low voltage applications.

A prototype micro-battery has been fabricated on a silicon wafer. Various passivation layers to protect the underlying devices and circuits have been evaluated. The most appropriate one is plasma enhanced chemical vapor deposited (PECVD) silicon oxynitride layer. This layer is impervious to the diffusion of lithium as confirmed by SIMS analysis. For the micro-battery, the cathode contact is evaporated chromium, which adheres well to the oxynitride layer and is already widely accepted in the IC industry for photolithography mask and as a barrier metal for solder bump. The cathode is TiS_2, which is sputtered from a composite target and is commonly used as a rechargeable electrode in thick film solid state batteries. The solid electrolyte is sputtered 6LiI-4Li3PO4-P2S5. The anode is evaporated lithium, and no anode cap is used in this first experiment. The sample therefore has to be stored and tested in an argon ambient to prevent oxidation. The micro-battery provides a voltage of 2V and a charge capacity of about 0.1C. The charging and discharging characteristics remain stable even after 1000 cycles.

Various prototype CMOS circuits suitable for integration with the micro-battery have been designed. These include circuitry for monitoring the status of the battery, charging and loading the battery, as well as typical low voltage analog (e.g., operational amplifier) and digital (e.g., ring oscillator) components. The prototype wafers have been fabricated and the circuits tested functional.

This project was terminated after two years due to budgetary limitations and the recommendation of the JSEP TCC. The original objectives of further improving the micro-battery and integrating the micro-battery with circuits could not be carried out.

3.6 Applications of Silicon-Germanium and Germanium Films in MOS Technologies

Scientific Objective

SiGe alloys combined with Si have provided a foundation to build heterojunction and quantum well devices in a Si based technology. The specific objectives of this project include the following:

- Fabrication of MODFET structures in strained $Si_{0.50}Ge_{0.50}$ on strain-relaxed $Si_{0.25}Ge_{0.75}$.
- Fabrication of MODFET structures in strained Ge on strain-relaxed $Si_{0.25}Ge_{0.75}$.
- Comparison of transport parameters of electrons confined through strain-induced degeneracy-splitting of the X-valleys ($Si_{0.50}Ge_{0.50}$ channel devices) with electrons confined through chemical energy-reduction in the L-valleys (Ge channel devices).
- Assess the utility of high-Ge content MODFETs in high-speed transistor applications, such as; data-sampling units, real-time signal processing, etc.
- Fabrication of MODFET structures in strained $Si_{0.50}Ge_{0.50}$ on strain-relaxed $Si_{0.25}Ge_{0.75}$.
- Fabrication of MODFET structures in strained Ge on strain-relaxed $Si_{0.25}Ge_{0.75}$.
- Comparison of transport parameters of electrons confined through strain-induced degeneracy-splitting of the X-valleys ($Si_{0.50}Ge_{0.50}$ channel devices) with electrons confined through chemical energy-reduction in the L-valleys (Ge channel devices).
- Assess the utility of high-Ge content MODFETs in high-speed transistor applications, such as; data-sampling units, real-time signal processing, etc.

Summary of Research

N-channel field effect transistors were formed in strain-relieved crystaling Ge deposited on Si substrates using graded-alloy epitaxy for accommodation of the 4% lattice mismatch between Ge and Si.

Using silane and germane sources, the alloy was linearly graded from pure silicon to pure germanium over approximately three micrometers of film thickness. A 0.5 micrometer cap was then grown for formation of the devices. The gate dielectric was formed via the chemical vapor deposition of SiO_2 using silane and oxygen at 400°C. An anneal in oxygen at 550°C formed

GeO_2 at the interface for improved interfacial quality. Sputtered aluminum was used for the gate. The source and drain were implemented through As implantation.

Extracted channel mobilities of near 300 cm^2/volt-second were observed. The extrapolated low-field mobility is near 550 cm^2/volt-second. The bulk mobility in germanium at room temperature is approximately 3000 cm^2/volt second. The reduction in the low-field mobility from this value is likely due to the Colombic scattering from the interface states. The interface state density was estimated at 1 x $10^{12}/cm^2$-eV near midgap and approximately 2.5 x $10^{12}/cm^2$-eV near the conduction band edge, 0.35 eV above midgap.

Only with improvement in the quality of the dielectric-semiconductor interface can the potential of germanium field-effect devices be properly realized. However, graded-alloy chemical vapor deposition was clearly shown to be an effective means of creating device-grade germanium on silicon substrates.

4. Information Systems

4.1 Portable Video on Demand in Wireless Communications

Scientific Objective

The goal of this research is to design a portable video-on-demand system capable of delivering high-quality image and video data in a wireless communication environment.

Summary of Research

The research focused on both the algorithm and circuit design techniques developed for implementing a low-power video compression/decompression system at power levels that are two orders of magnitude below existing solutions. This low-power video compression system not only provides a compression efficiency similar to industry standards, but also maintains a high degree of error tolerance to guard against transmission errors often encountered in wireless communication.

The required power reduction can best be attained through reformulating compression algorithms for energy conservation. We developed an intra-frame compression algorithm that requires minimal computation energy in its hardware implementations. Examples of algorithmic trade-offs are the development of a vector quantization scheme that allows on-chip computation to eliminate off-chip memory accesses, the use of channel-optimized data representations to avoid the error control hardware that would otherwise be necessary, and the coding of internal data representations to further reduce the energy consumed in data exchanges. The architectural and circuit design techniques used include the selection of a filter

bank structure that minimizes the energy consumed in the datapath, the data shuffle strategy that results in reduced internal memory size, and the design of digital and analog circuits optimized for low supply voltages.

Our hardware prototype is a video decoding chip set for decompressing full-motion video transmitted through a wireless link at less than 10 mW, which is incorporated into a hand-held portable communication device with a color display.

4.2 Wireless Data Transmission Fundamentals

Scientific Objectives

Digital wireless transmission has rapidly become commonplace over the past five years and increasing numbers of users with higher bandwidths begins to stress current and even contemplated implementations. The objective of this research is to determine and compute bounds for highest data rate transmission achievable in fixed and portable wireless digital transmission environments, as well as to derive system architectures that would allow these limits to be achieved.

Summary of Research

The work has produced two fundamental methods that significantly advance the body of knowledge in the area of wireless transmission. The first is the area of super-redundant codes by Rick Wesel and of Vector-OFDM transmission methods by Greg Raleigh.

Super-redundant codes:

Rick Wesel's thesis and related publications address the problem of optimizing transmission code with a known fixed used spectrum for transmission on a point-to-point transmission link. This problem required significant work to pose correctly for the various impairments of wireless transmission, namely time-varying, unknown, frequency-selective Raleigh (as in Lord Raleigh, not to be confused with Greg Raleigh) fading. This work found a new class of codes and design criteria/procedures that are tuned to the wireless opportunity, producing a number of codes that allow the highest data rates to be obtained on a wireless point-to-point link.

Vector OFDM:

Greg Raleigh's thesis and related publications address both the problems of computing the maximum possible number of bits that can be transmitted per second per unit of volume. It is the recognition of the "per volume" constraint, that allows much higher data rates to be achieved in wireless communications that is fundamental. The improvements can be orders of

magnitude. Raleigh then proceeded to derive a method that allows these fundamental rates to be nearly achieved, which is vector OFDM. Vector OFDM uses adaptively steered transmit and receive antenna arrays. At each point in space, a user receives only signals intended for him and is zero at all other points in space where other receivers might exist. The complexity of this approach is very high and is now being investigated by other current Stanford students.

4.3 Smart Antennas for Mobile Radio Networks

Scientific Objective:

The objective of this project was to investigate the potential to improve both military and civilian mobile radio networks through exploitation of spatial structure and signal structure in smart antennas. These investigations covered three specific areas: (I) Spatio-Temporal Blind Identification of FIR Channels for Multiple Users, (ii) Closed-Form Solutions to the Constant-Modulus Factorization Problem, and (iii) Blind Adaptive Demodulation of Co-channel FM Signals.

Summary of Research

We found that using smart antennas at the network base station can substantially improve the capacity (number of users per cell) and quality (outage probability) of such networks.

A second effort was the study of the robustness of algorithms with respect to rapid time-variations and underlying model uncertainties in the urban mobile communications environment. Of particular interest were adaptive filtering algorithms which are widely used in mobile communications (as well as in many other areas) for the identification and equalization of channels. In this regard, we focused on the so-called H^∞ approach to robust estimation and control, and demonstrated that the celebrated LMS (least-mean-squares) adaptive filtering algorithm is H^∞-optimal. Other results in this area have been reported in the annual report for this period, and include the study of various forms of estimation errors, robustness of least-squares algorithms, and time-variant problems.

Finally, our attention focused on (so-called) mixed H^2/H^∞ estimators and adaptive filters. Briefly, the mixed H^2/H^∞ approach to estimation attempts to achieve a tradeoff between the following two approaches:

- The H^2 approach that has the best average performance, under the assumption of perfect modes and complete knowledge of the statistics of the exogenous signal. This approach, however, has the drawback of being nonrobust with respect to modeling

errors and disturbance uncertainty.

- The H^∞ approach that has the best worst-case performance and is therefore robust with respect to model uncertainty and lack of statistical information on the exogenous signals. The drawback of this approach is that it may be over-conservative.

More explicitly, the mixed H^2/H^∞ approach is concerned with the design of estimators that have the best average performance, not over the set of all estimators, but over a restricted set that guarantees a certain worst-cast performance bound. This approach therefore strikes a balance between the two extremes of H^2 and H^∞ estimation and should be of great practical significance in situations (such as mobile communications) where the precise models and statistics are not completely known or are to expensive to obtain.

Unlike the H^2 and H^∞ problems, the question of finding the optimal mixed H^2/H^∞ estimator has been an open problem. We showed for the first time, how to construct the optimal mixed H^2/H^∞ estimator for adaptive filtering. The resulting estimator is nonlinear and has the best least-mean-squares (or average) performance over all estimators that achieve the optimal H^∞ (or worst-case) bound. Moreover, the algorithm require $O(n^2)$ operations per iteration, where n is the number of weights in the adaptive filter, which is the same order of complexity required of the standard H^2 and H^∞ optimal estimators. Simulation studies have also been performed to compare the performance of the mixed H^2/H^∞ adaptive filter, with standard least-squares and H^∞ adaptive filters. Finally, extensions to general estimation problems have been studied.

4.4 Efficient Data Compression

Scientific Objectives

We apply techniques of information theory to problems of information compression, image compression, distributed data compression and storage and network information flow. This includes investigation of techniques for lossy and noiseless data compression using arithmetic coding and Kolmogorov complexity.

Summary of Research

We have run an experiment to find the rate distortion function for images. There are existing algorithms — JPEG, for example – which compress images. However, it is clear that computers can't "see", while humans can. Thus we expect that humans compress images better than computers and we want to know how much better. We have designed an experiment for noisy image compression with human intervention which outperforms JPEG by a factor of two. This bound on achievable compression shows that substantial improvement over current schemes is possible. However, we were only able to achieve this factor of two improvement by using an algorithm that takes roughly 100 hours of human interaction per image. Now that we know how well we can do, steps can be taken to make this algorithm automatic and efficient.

In related work, we have applied the literature on universal data compression (data compression algorithms that are good regardless of the source) to portfolio theory. We have shown a precise mathematical similarity between the description rate in data compression and the growth rate of wealth in investing in the stock market. This should lead to algorithms of great economic importance, not only in investment, but in allocation of resources in all processes which have an exponential growth rate associated with them.

Finally, in a series of papers, Lapidoth has established the robustness of codes for Gaussian noise environments. Current modulation schemes for code division multiple access in mobile communications are designed to work well when the ambient noise and interference is Gaussian. We have been able to show that these signaling schemes will work even better (have a lower probability of error and a lower distortion) if the noise is non-Gaussian. In other words, Gaussian noise is the worst case, and designing for the worst case will guarantee that one does even better when the Gaussian noise assumption is violated. This robustness is not only reassuring, but is important when the interference and noise is due to jamming. The communication systems remains invulnerable.

5. JSEP Supported Dissertations

1. B. M. Gordon, "Low-Power Video Compression for Portable Applications using Subband Coding," Ph.D. Thesis, Stanford University, June 1996.
2. E. K. Tsern, "Error Resilient Video Compression for Portable Applications using Pyramid Vector Quantization," Ph.D. Thesis, Stanford University, June 1996.
3. C. I. Duruöz, "Low Temperature Transport in Quantum Dot Arrays," Ph.D. Thesis, Stanford University, April 1996.
4. J. C. Beckman, "Low-Current Emission Characteristics of Liquid Metal Ion Sources," Ph.D. Thesis, Stanford University, June 1997.
5. T. H. Chung, "Minimax Learning in Iterated Games via Distributional Majorization," Ph.D. Thesis, Stanford University, August 1994.
6. V. Castelli, "The Relative Value of Labeled and Unlabeled Samples in Pattern Recognition," Ph.D. Thesis, Stanford University, December 1994.
7. J. P. Snyder, "The Physics and Technology of Platinum Silicide Source and Drain Field Effect Transistors," Ph.D. Thesis, Stanford University, March 1996.

8. D. S. Marshall, "Doping Study of High Temperature Superconductors Using Angle-Resolved Photo-Electron Spectroscopy," Ph.D. Thesis, Stanford University, April 1996.
9. B. Hassibi, "Indefinite Metric Spaces in Estimation, Control and Adaptive Filtering, Ph.D. Thesis, Stanford University, 1996.

6. JSEP Supported Publications

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2. B. M. Gordon, T. H. Meng, "A 1.2mW Video-Rate 2D Color Subband Decoder," *Digest of Technical Papers*, 1995 IEEE International Solid-State Circuits Conference, pp. 290-291, February 1995.
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9. C. M. Marcus, R. M. Clarke, I. H. Chan, C. I. Duruöz and J. S. Harris, "Phase-breaking rates from conductance fluctuations in a quantum dot," *Semiconductor Science and Technology* **9**, 1897-1901.
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